IN THE CLAIMS

Please amend claims as follows:

1. (Currently amended) A method for performing a processing function ~~of a memory~~ in a block memory, wherein said block memory comprises ~~comprising~~ memory cells for storing data~~, where data can be stored,~~ and a connection bus comprising at least a ready/busy line, which can be set at least to a ready status and to a busy status, said method comprising

setting the status of said ready/busy line to said busy status in a beginning of the processing function,

performing detection of processing errors,

indicating an end of the processing function by setting said ready/busy line to said ready status, and

changing the status of said ready/busy line back to said busy status if a processing error is detected.

2. (Currently amended) The method according to claim 1, wherein said processing function is erasing the block memory ~~is used as said processing function~~, and performing detection of processing errors comprises ~~the method comprising~~

performing a comparison of an erased memory cell with the data meant for the status of the erased memory cell in connection with erasing, ~~in order to detect erasing errors~~, and wherein

if an erasing error is detected in the comparison, ~~changing~~ the status of said ready/busy line is changed back to said busy status.

3. (Currently amended) The method according to claim 1, wherein said processing function is storing data to the block memory ~~is used as said processing function~~, and performing detection of processing errors comprises ~~the method comprising~~

performing a comparison of stored data with data meant to be stored in connection with storing the data, ~~in order to detect storing errors,~~ and

wherein if a storing error is detected in the comparison, ~~changing~~ the status of said ready/busy line is changed back to said busy status.

4. (Currently amended) The method according to claim 1, wherein said processing function is copying data in the block memory from one location to some other location ~~is used as said processing function~~, and performing detection of processing errors comprises ~~the method comprising~~

performing a comparison of copied data with data meant to be copied in connection with copying the data~~, in order to detect copying errors~~, and

wherein if a copying error is detected in the comparison, ~~changing~~ the status of said ready/busy line is changed back to said busy status.

5. (Currently amended) The method according to claim 1, wherein said processing function is reading data from the block memory ~~is used as said processing function~~, and performing detection of processing errors comprises ~~the method comprising~~

performing examining status of a memory cell being read in connection with reading data, and

wherein if a memory cell error is detected in the examination, ~~changing~~ the status of said ready/busy line is changed back to said busy status.

6. (Original) The method according to claim 1, comprising

starting the processing function by sending a command to the block memory, and

setting the status of said ready/busy line to the busy status in a stage when a function according to the command is started in the block memory.

7. (Original) The method according to claim 1, wherein the block memory is divided into blocks, and each block is divided into pages, the method comprising

transmitting data to the block memory page by page.

8. (Original) The method according to claim 7, comprising

performing erasing of at least one block, and

setting a previously determined status as the status of all the memory cells of said at least one block.

9. (Original) The method according to claim 1, comprising

examining the status of said ready/busy line, and

performing re-examination of the status of the ready/busy line when it changes from the busy status to the ready status.

10. (Original) The method according to claim 1, wherein the connection bus comprises a data bus comprising at least one data line, the method comprising

using the data line of said data bus as a ready/busy line.

11. (Currently amended) A system, ~~which comprises~~comprising

an electronic device comprising a block memory having ~~comprising~~ memory cells for storing data, and a connection bus connected to said block memory,

wherein said connection bus comprises ~~comprising~~ at least a ready/busy line~~,~~ ~~and~~capable of indicating

at least a ready status and a busy status ~~are defined for said ready/busy line~~, and

~~which~~ wherein said block memory comprises

means for changing the status of said ready/busy line to said busy status in ~~the~~ a beginning of ~~the~~ a processing function of the block memory,

a comparator for detecting processing errors, ~~and~~

means for indicating the end of processing function by setting said ready/busy line to said ready status, and

~~the system further comprising~~

means for changing the status of said ready/busy line back to said busy status after detecting a processing error.

12. (Currently amended) The system according to claim 11, wherein said processing function is one of the following:

emptying the memory cells,
storing data in the memory cells,
copying data between the memory cells,
reading ~~the~~ data stored in the memory cells.

13. (Original) The system according to claim 11, comprising a processor, and a first connection bus between the processor and the block memory, and means for starting the processing function by sending a command to the block memory, and means for setting the status of said ready/busy line to the busy status when the function according to the command has been started in the block memory.

14. (Original) The system according to claim 13, comprising means for creating an interrupt in the processor when the status of the ready/busy line changes from the busy status to the ready status, and the processor comprising means for examining the status of the ready/busy line in connection with handling the interrupt.

15. (Original) The system according to claim 11, comprising a processor, a memory controller, a first connection bus between the processor and the memory controller, and a second connection bus between the memory controller and the block memory, in which case the commands are arranged to be sent from the processor to the memory controller, as well as from the memory controller to the block memory, the system comprising means for starting storing of the data by sending a command to the block memory, and means for setting the status of said ready/busy line to the busy status when the function according to the command has been started in the block memory.

16. (Original) The system according to claim 15, comprising means for creating an interrupt in the memory controller when the status of the ready/busy line changes from the busy status to the ready status, wherein the memory controller comprises means for examining the status of the ready/busy line in connection with handling the interrupt, and means for forming an interrupt to the processor if the ready/busy line is in the busy status.

17. (Original) The system according to claim 11, wherein the block memory is divided into blocks, and each block is divided into pages, the system comprising means for transmitting data to the block memory page by page.

18. (Original) The system according to claim 11, the bus interface comprising a data bus comprising at least one data line, and that the data line of said data bus is arranged to be used as a ready/busy line.

19. (Currently amended) An electronic device, ~~which comprises~~comprising a block memory ~~comprising~~ having memory cells for storing data, and a bus interface connected to said block memory,

wherein said connection bus comprises ~~comprising~~ at least a ready/busy line capable of indicating ~~and~~ at least a ready status and a busy status ~~are defined for said ready/busy line~~,

and wherein said ~~which~~ block memory comprises

means for setting the status of said ready/busy line to said busy status in ~~the~~ a beginning of a processing function of the block memory,

a comparator for detecting processing errors, ~~and~~

means for indicating an end of the processing function by setting said ready/busy line to said ready status, and

~~the electronic device further comprising~~ means for changing the status of said ready/busy line back to said busy status after detecting a processing error.

20. (Currently amended) A block memory, comprising

memory cells for storing data, and

a connection bus comprising at least a ready/busy line, capable of indicating ~~and~~ at least a ready status and a busy status ~~are defined for said ready/busy line~~, ~~and~~

~~which~~ wherein said block memory further comprises

means for setting the status of said ready/busy line to said busy status in a beginning of a processing function of the block memory,

a comparator for detecting processing errors, ~~and~~

means for indicating an end of processing function by setting said ready/busy line to said ready status, and

~~the block memory further comprising~~ means for changing the status of said ready/busy line back to said busy status after detecting a processing error.

21. (Currently amended) The memory block according to claim 20, wherein said processing function is one of the following:

emptying the memory cells,

storing data in the memory cells,

copying data between the memory cells, and

reading ~~the~~ data stored in the memory cells.

22. (Original) The block memory according to claim 20, comprising a comparator for comparing the data stored in the memory cells with data meant to be stored in order to detect storing errors.